



ALPHA & OMEGA
SEMICONDUCTOR, LTD



AOD407

P-Channel Enhancement Mode Field Effect Transistor

General Description

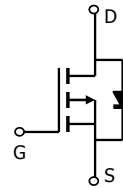
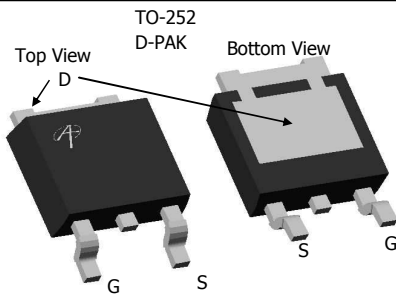
The AOD407 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and low gate resistance. With the excellent thermal resistance of the DPAK package, this device is well suited for high current load applications.

- RoHS Compliant
- Halogen Free*

Features

- $V_{DS} (V) = -60V$
- $I_D = -12A (V_{GS} = -10V)$
- $R_{DS(ON)} < 115m\Omega (V_{GS} = -10V)$
- $R_{DS(ON)} < 150m\Omega (V_{GS} = -4.5V)$

UIS TESTED!
Rg, Ciss, Coss, Crss Tested



Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

| Parameter | Symbol | Maximum | Units |
|--|----------------|-------------------|------------|
| Drain-Source Voltage | V_{DS} | -60 | V |
| Gate-Source Voltage | V_{GS} | ± 20 | V |
| Continuous Drain Current ^G | I_D | $T_C=25^\circ C$ | -12 |
| | | $T_C=100^\circ C$ | -10 |
| Pulsed Drain Current ^C | I_{DM} | -30 | A |
| Avalanche Current ^C | I_{AR} | -12 | A |
| Repetitive avalanche energy $L=0.1mH$ ^C | E_{AR} | 23 | mJ |
| Power Dissipation ^B | P_D | $T_C=25^\circ C$ | 50 |
| | | $T_C=100^\circ C$ | 25 |
| Power Dissipation ^A | P_{DSM} | $T_A=25^\circ C$ | 2.5 |
| | | $T_A=70^\circ C$ | 1.6 |
| Junction and Storage Temperature Range | T_J, T_{STG} | -55 to 175 | $^\circ C$ |

Thermal Characteristics

| Parameter | Symbol | Typ | Max | Units |
|--|-----------------|--------------|-----|--------------|
| Maximum Junction-to-Ambient ^A | $R_{\theta JA}$ | 16.7 | 25 | $^\circ C/W$ |
| Maximum Junction-to-Ambient ^A | | Steady-State | 40 | 50 |
| Maximum Junction-to-Case ^B | $R_{\theta JC}$ | 2.5 | 3 | $^\circ C/W$ |

Electrical Characteristics (T_J=25°C unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|-----------------------------|---------------------------------------|--|------|--------|------|-------|
| STATIC PARAMETERS | | | | | | |
| BV _{DSS} | Drain-Source Breakdown Voltage | I _D =-250μA, V _{GS} =0V | -60 | | | V |
| I _{DSS} | Zero Gate Voltage Drain Current | V _{DS} =-48V, V _{GS} =0V T _J =55°C | | -0.003 | -1 | μA |
| I _{GSS} | Gate-Body leakage current | V _{DS} =0V, V _{GS} =±20V | | | ±100 | nA |
| V _{GS(th)} | Gate Threshold Voltage | V _{DS} =V _{GS} I _D =-250μA | -1.5 | -2.1 | -3 | V |
| I _{D(ON)} | On state drain current | V _{GS} =-10V, V _{DS} =-5V | -30 | | | A |
| R _{DS(ON)} | Static Drain-Source On-Resistance | V _{GS} =-10V, I _D =-12A T _J =125°C | | 91 | 115 | mΩ |
| | | V _{GS} =-4.5V, I _D =-8A | | 114 | 150 | mΩ |
| g _{FS} | Forward Transconductance | V _{DS} =-5V, I _D =-12A | | 12.8 | | S |
| V _{SD} | Diode Forward Voltage | I _S =-1A, V _{GS} =0V | | -0.76 | -1 | V |
| I _S | Maximum Body-Diode Continuous Current | | | | -12 | A |
| DYNAMIC PARAMETERS | | | | | | |
| C _{iss} | Input Capacitance | | | 987 | 1185 | pF |
| C _{oss} | Output Capacitance | V _{GS} =0V, V _{DS} =-30V, f=1MHz | | 114 | | pF |
| C _{rss} | Reverse Transfer Capacitance | | | 46 | | pF |
| R _g | Gate resistance | V _{GS} =0V, V _{DS} =0V, f=1MHz | | 7 | 10 | Ω |
| SWITCHING PARAMETERS | | | | | | |
| Q _g (10V) | Total Gate Charge (10V) | | | 15.8 | 20 | nC |
| Q _g (4.5V) | Total Gate Charge (4.5V) | V _{GS} =-10V, V _{DS} =-30V, I _D =-12A | | 7.4 | 9 | nC |
| Q _{gs} | Gate Source Charge | | | 3 | | nC |
| Q _{gd} | Gate Drain Charge | | | 3.5 | | nC |
| t _{D(on)} | Turn-On DelayTime | | | 9 | | ns |
| t _r | Turn-On Rise Time | V _{GS} =-10V, V _{DS} =-30V, R _L =2.5Ω, | | 10 | | ns |
| t _{D(off)} | Turn-Off DelayTime | R _{GEN} =3Ω | | 25 | | ns |
| t _f | Turn-Off Fall Time | | | 11 | | ns |
| t _{rr} | Body Diode Reverse Recovery Time | I _F =-12A, dI/dt=100A/μs | | 27.5 | 35 | ns |
| Q _{rr} | Body Diode Reverse Recovery Charge | I _F =-12A, dI/dt=100A/μs | | 30 | | nC |

A: The value of R qJA is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with T A =25°C. The Power dissipation PDSM is based on R qJA and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B: The power dissipation PD is based on T_J(MAX)=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature T_J(MAX)=175°C.

D: The R qJA is the sum of the thermal impedance from junction to case R qJC and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using <300 ms pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_J(MAX)=175°C.

G: The maximum current rating is limited by bond-wires.

H: These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with TA=25°C. The SOA curve provides a single pulse rating.

*This device is guaranteed green after data code 8X11 (Sep f^T 2008).

Rev 6 : Sep 2008

THIS PRODUCT HAS BEEN DESIGNED AND QUALIFIED FOR THE CONSUMER MARKET. APPLICATIONS OR USES AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

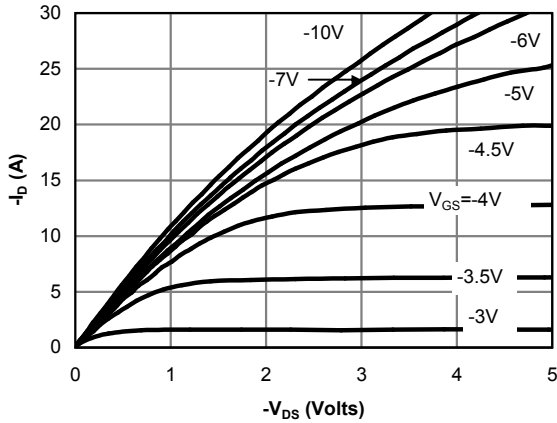


Fig 1: On-Region Characteristics

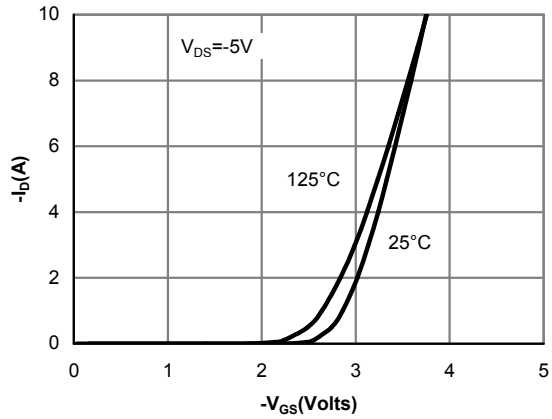


Figure 2: Transfer Characteristics

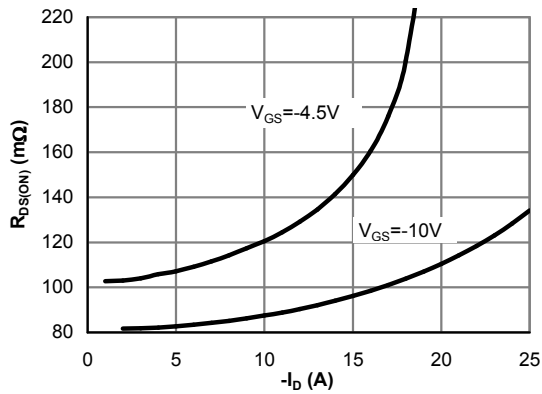


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

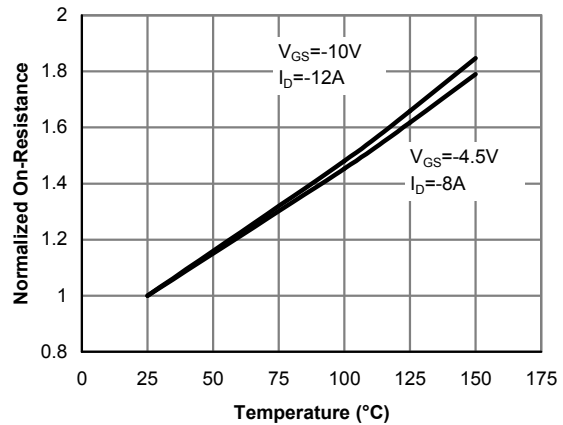


Figure 4: On-Resistance vs. Junction Temperature

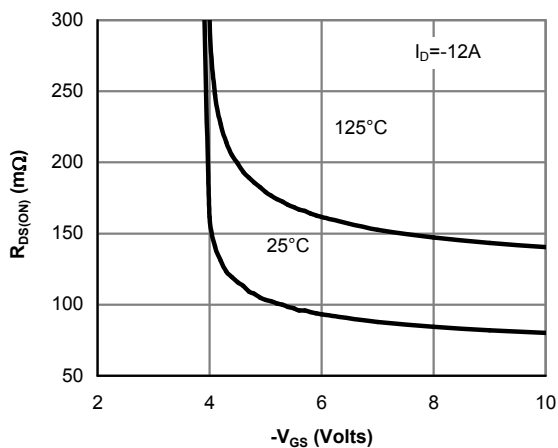


Figure 5: On-Resistance vs. Gate-Source Voltage

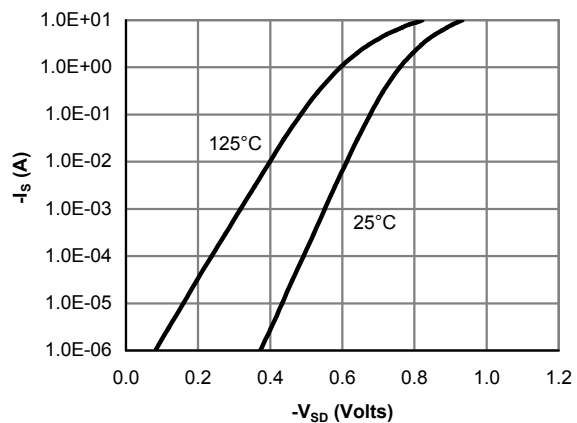


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

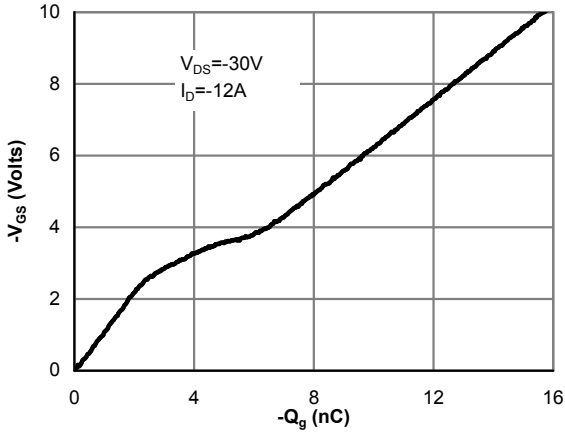


Figure 7: Gate-Charge Characteristics

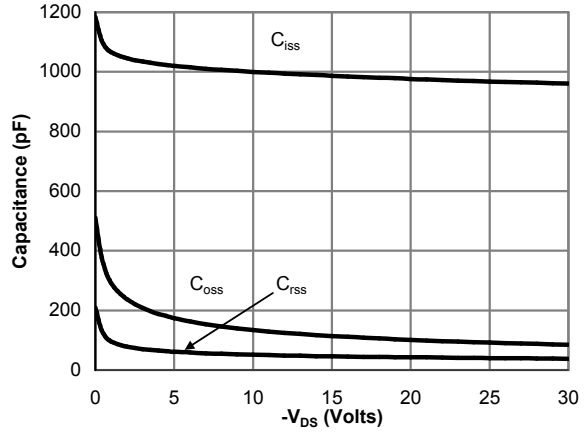


Figure 8: Capacitance Characteristics

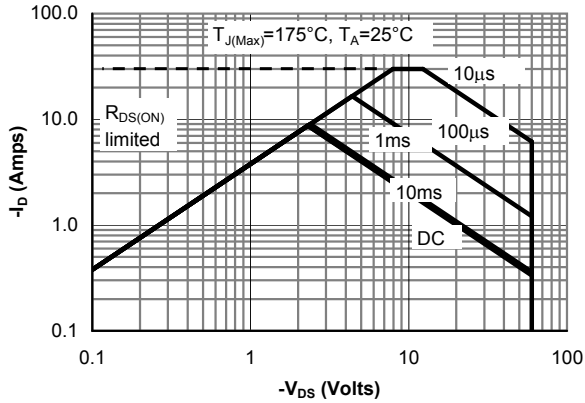


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

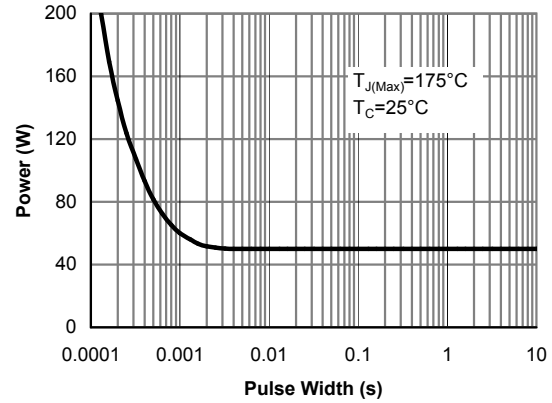


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

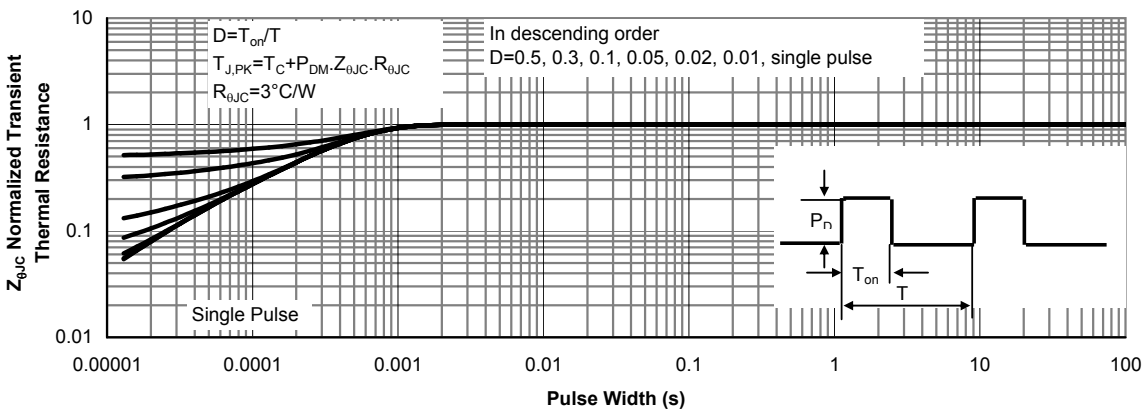


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

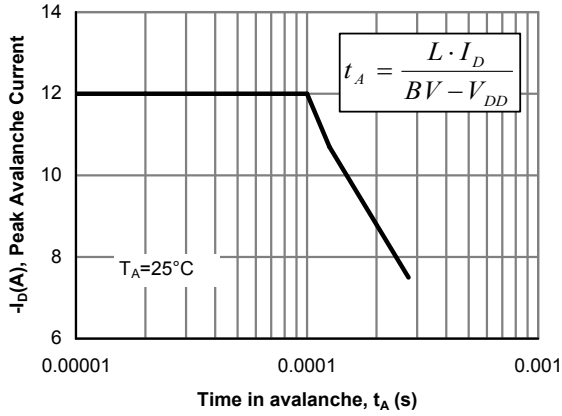


Figure 12: Single Pulse Avalanche capability

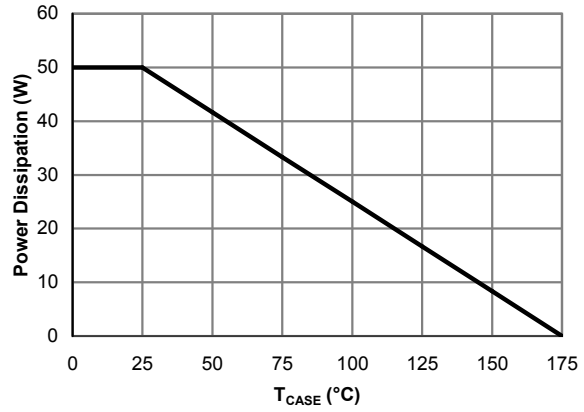


Figure 13: Power De-rating (Note B)

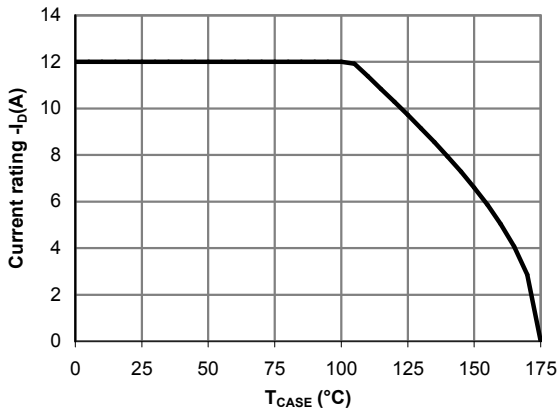


Figure 14: Current De-rating (Note B)

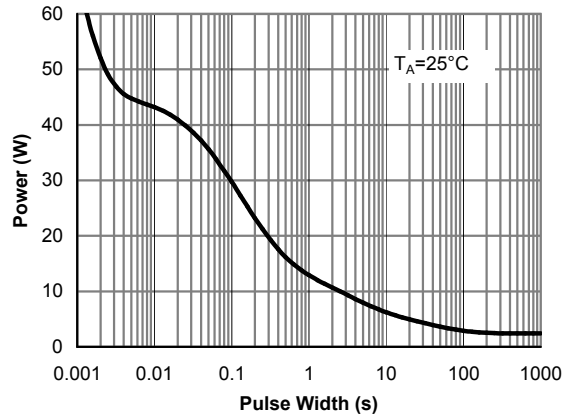


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

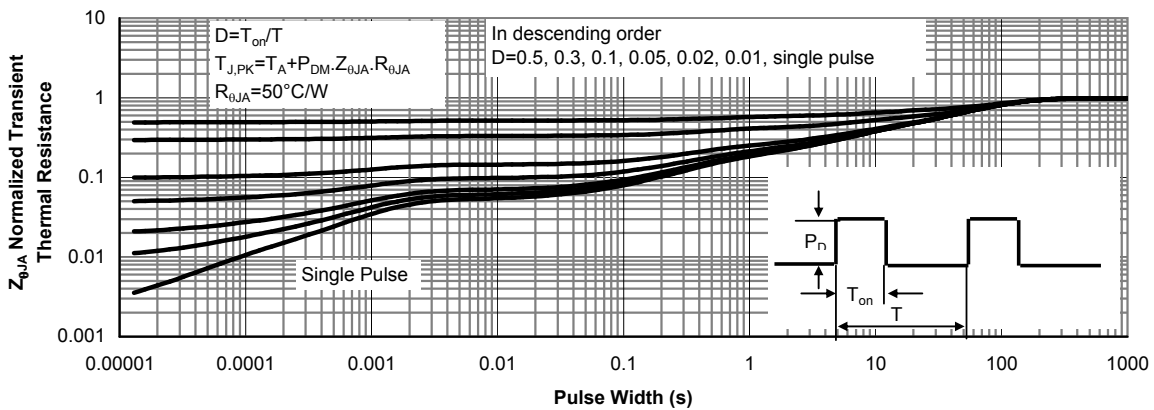
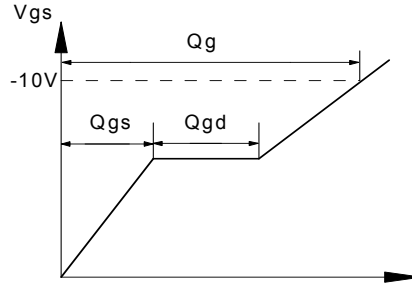
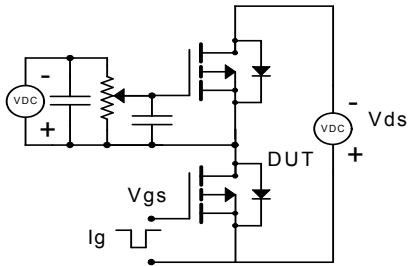
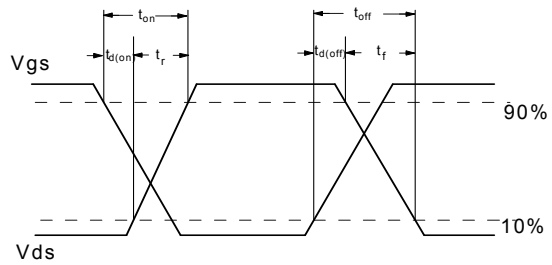
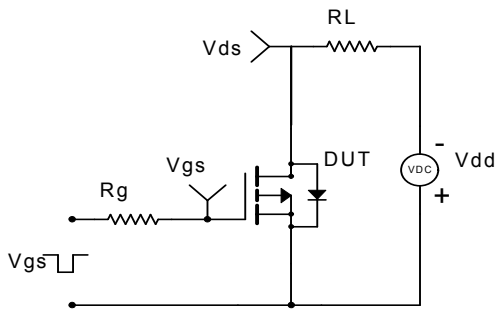


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

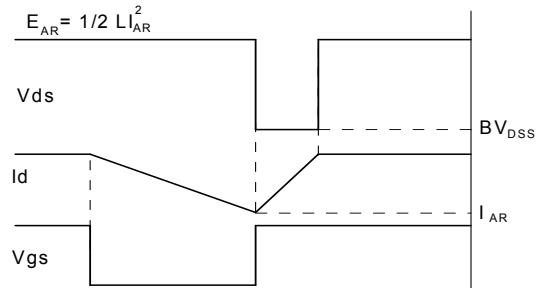
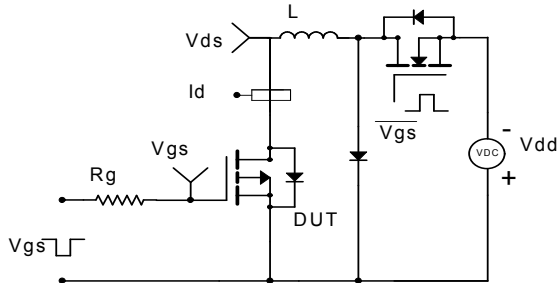
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

